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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
09/996,574	11/30/2001	Shigeki Tomishima	57454-309	3797

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EXAMINER
MANDALA, VICTOR A

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No.	Applicant(s)
09/996,574	TOMISHIMA, SHIGEKI
Examiner	**Art Unit**
Victor A Mandala Jr.	2826

Office Action Summary

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *3 and 8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7 and 9-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2001* is/are. a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*
4)☐ Interview Summary (PTO-413) Paper No(s) _____
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other

DETAILED ACTION

Election/Restrictions

1. Examiner has noted that the applicant has responded to the election restriction from the last communication response filed on 8/26/02. The applicant has elected Species I, of Figures 1-13, claims 1-2, 4-7, and 9-11 for further examination with traverse. Examiner has considered applicants' arguments and the initial election of Species II, Figure 14, and Species III, Figure 15 and 16, was appropriate. Examiner makes election of Species I, of Figures 1-13, final.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the metal interconnection line is a copper interconnection line must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. The drawings show the metal interconnection line being made of an aluminum interconnection line.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-2, 4-7, and 9-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. The expression electrically connected to the corresponding sub word line to define the role of said shunting interconnection lines is not clear since it is unknown if signals are supplied by said shunting lines or not.

4. The expression sub word lines indicates word lines having associated sub word lines with them. This concept makes it unclear which lines: the word lines as known by the art of said sub lines are the actual word lines of the memory matrix. To the alternative, it is not clear if said sub word lines are the actual word lines of the matrix. If there are word lines and sub word lines in the matrix, then the applicant must present how they function in tandem.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-2, 4-7, and 9-10 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,240,006 Kawasaki, (insofar as to understand the claims as stated in the above 35 U.S.C 112 2nd paragraph rejection).

5. Referring to claim 1, a semiconductor memory device comprising: a plurality of memory cells arranged in rows and columns: a plurality of sub word lines, provided corresponding to the respective memory cell rows, each having memory cells on a corresponding row connected thereto: a plurality of main word lines, each provided corresponding to a prescribed number of sub word lines in said plurality of sub word lines, (Col. 8 Lines 40-49), and disposed in a first conductive layer, (Figure 7 #10 & Col. 10 Lines 24-27), for transmitting a row select signal, (Figure 7 #10 & Col. 10 Lines 24-27): a plurality of shunting interconnection lines, (Figure 7 #43 & Col. 12 Lines 56-58), provided corresponding to the respective sub word lines in a second conductive layer formed under said first conductive layer, (Figure 7 #43 & Col. 12 Lines 56-58), each for electrically connecting to a corresponding sub word line at a prescribed interval: and a

plurality of sub word drivers, provided corresponding to the sub word lines. (Figure 7 #10 & Col. 10 Lines 24-27), each for driving a corresponding sub word line and a corresponding shunting interconnection line into a selected state according to at least a row select signal on a corresponding main word line. (Col. 1 Lines 28-31 & Col. 2 Lines 45-52).

6. Referring to claim 2, a semiconductor memory device, wherein said first conductive layer, (Figure 7 #10), is a third level metal interconnection layer, (Figure 7 #10), and said second conductive layer, (Figure 7 #43), is a first level metal interconnection layer, (Figure 10 #43).

7. Referring to claim 4, a semiconductor memory device, further comprising an intermediate voltage transmission line, formed in a third conductive layer different from the first and second conductive layers, for transmitting an intermediate voltage at a prescribed voltage level. (Col. 18 Lines 49-60).

8. Referring to claim 5, a semiconductor memory device, wherein
said third conductive layer is a second level metal interconnection line formed in an interconnection layer between the first and second conductive layers. (Col. 18 Lines 49-60).

9. Referring to claim 6, a semiconductor memory device, wherein each memory cell has a capacitance for storing information and said intermediate voltage is applied to a reference power supply node of said capacitance. (Col. 12 Lines 60-65).

10. Referring to claim 7, a semiconductor memory device, wherein said reference power supply node is formed under said second conductive layer, said third conductive layer is electrically connected to said reference power supply node through a metal interconnection line formed in said second conductive layer. (Col. 13 Lines 11-20).

11. Referring to claim 9, a semiconductor memory device, further comprising a power supply line, disposed in an interconnection layer different from said first conductive layer over a memory cell array in which said plurality of memory cells are arranged, for transmitting a power supply voltage, (Col. 18 Lines 49-60).

12. Referring to claim 10, a semiconductor memory device, wherein said semiconductor memory device is an embedded memory integrated with a logic circuit on a common semiconductor substrate, (Col. 19 Lines 33-37).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-7, and 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Patent No. 11-354745 Kawasaki, (insofar as to understand the claims as stated in the above 35 U.S.C 112 2nd paragraph rejection & using U.S. Patent No. 6,240,006 Kawasaki, which claims priority of the Japanese Patent No. 11-354745 Kawasaki is used as the English translation).

13. Referring to claim 1, a semiconductor memory device comprising: a plurality of memory cells arranged in rows and columns; a plurality of sub word lines, provided corresponding to the respective memory cell rows, each having memory cells on a corresponding row connected

thereto: a plurality of main word lines, each provided corresponding to a prescribed number of sub word lines in said plurality of sub word lines, (Col. 8 Lines 40-49), and disposed in a first conductive layer, (Figure 7 #10 & Col. 10 Lines 24-27), for transmitting a row select signal, (Figure 7 #10 & Col. 10 Lines 24-27); a plurality of shunting interconnection lines, (Figure 7 #43 & Col. 12 Lines 56-58), provided corresponding to the respective sub word lines in a second conductive layer formed under said first conductive layer, (Figure 7 #43 & Col. 12 Lines 56-58), each for electrically connecting to a corresponding sub word line at a prescribed interval; and a plurality of sub word drivers, provided corresponding to the sub word lines, (Figure 7 #10 & Col. 10 Lines 24-27), each for driving a corresponding sub word line and a corresponding shunting interconnection line into a selected state according to at least a row select signal on a corresponding main word line, (Col. 1 Lines 28-31 & Col. 2 Lines 45-52).

12. Referring to claim 2, a semiconductor memory device, wherein said first conductive layer, (Figure 7 #10), is a third level metal interconnection layer, (Figure 7 #10), and said second conductive layer, (Figure 7 #43), is a first level metal interconnection layer, (Figure 10 #43).

13. Referring to claim 4, a semiconductor memory device, further comprising an intermediate voltage transmission line, formed in a third conductive layer different from the first and second conductive layers, for transmitting an intermediate voltage at a prescribed voltage level, (Col. 18 Lines 49-60)

14. Referring to claim 5, a semiconductor memory device, wherein

said third conductive layer is a second level metal interconnection line formed in an interconnection layer between the first and second conductive layers, (Col. 18 Lines 49-60).

15. Referring to claim 6, a semiconductor memory device, wherein each memory cell has a capacitance for storing information and said intermediate voltage is applied to a reference power supply node of said capacitance, (Col. 12 Lines 60-65).

16. Referring to claim 7, a semiconductor memory device, wherein said reference power supply node is formed under said second conductive layer, said third conductive layer is electrically connected to said reference power supply node through a metal interconnection line formed in said second conductive layer, (Col. 13 Lines 11-20).

17. Referring to claim 9, a semiconductor memory device, further comprising a power supply line, disposed in an interconnection layer different from said first conductive layer over a memory cell array in which said plurality of memory cells are arranged, for transmitting a power supply voltage, (Col. 18 Lines 49-60).

18. Referring to claim 10, a semiconductor memory device, wherein said semiconductor memory device is an embedded memory integrated with a logic circuit on a common semiconductor substrate, (Col. 19 Lines 33-37).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese Patent No. 11-354745 Kawasaki in view of U.S. Patent No. 5,748,549 Kometani et al., (insofar as to understand the claims as stated in the above 35 U.S.C 112 2nd paragraph rejection & using U.S. Patent No. 6,240,006 Kawasaki, which claims priority of the Japanese Patent No. 11-354745 Kawasaki is used as the English translation).

19. Referring to claim 11, a semiconductor memory device, wherein the metal interconnection line is a copper interconnection line. (Kometani et al. Col. 4 Lines 10-12). Japanese Patent No. 11-354745 Kawasaki discloses the claimed invention except for the interconnection lines being made of copper, but Kometani et al.discloses the interconnection lines could be made of copper. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the interconnection lines out of copper instead of the published aluminum, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
September 16, 2002